What is claimed is:

1. An on-die termination ("ODT") circuit for use in a synchronous memory device, the ODT circuit comprising:

a termination voltage port for receiving a termination voltage;

a data input/output ("I/O") port;

a first termination resistor, one end of which is connected to the data I/O port; and

a switch that selectively connects the other end of the first termination resistor to the termination voltage port in response to a termination enable signal.

2. The ODT circuit of Claim 1, further comprising a termination enable signal generating circuit for generating the termination enable signal in response to a signal which indicates a valid section of input data or indicates that the present period is not a read period during write operations of the synchronous memory device, and for generating the termination enable signal in response to a signal output from a mode set register ("MRS").

3. The ODT circuit of Claim 2, wherein the termination enable signal is enabled when the signal output from the MRS is disabled and when the signal which indicates a valid section of the input data or indicates that the present period is not a read period is enabled.

4. The ODT circuit of Claim 2, wherein the termination enable signal is enabled when the signal output from the MRS is enabled, irrespective of the signal indicating an effective section of the input data or indicating that the present period is not a read period.

5. The ODT circuit of Claim 2, further comprising a second termination resistor, one end of which is connected to the data I/O port and the other end of which is connected to the termination voltage port.

6. The ODT circuit of Claim 5, wherein a resistance value of the second termination resistor is remarkably larger than that of the first termination resistor.

7. The ODT circuit of Claim 1, wherein the termination voltage is generated by a voltage regulator included in a system to which the synchronous memory device is attached.

8. The ODT circuit of Claim 1, wherein the termination voltage is generated by a memory controller included in a system to which the synchronous memory device is attached.

9. The ODT circuit of Claim 1, wherein there is at least one termination voltage port.

10. An ODT method for a synchronous memory device, the method comprising:

installing a termination voltage port in the synchronous memory device, the termination voltage port receiving a termination voltage;

installing a first termination resistor in the synchronous memory device, the first termination resistor having one end connected to a data I/O port in the synchronous memory device; and

selectively connecting the other end of the first termination resistor to the termination voltage port.

11. The ODT method of Claim 10, wherein selectively connecting the other end of the first termination resistor is performed in a valid section of input data during write operations of the synchronous memory device.

12. The ODT method of Claim 10, wherein selectively connecting the other end of the first termination resistor is performed in periods other than read operations of the synchronous memory device.

13. The ODT method of Claim 10, wherein selectively connecting the other end of the first termination resistor is performed when an MRS included in the synchronous memory device is set outside the synchronous memory device.

14. The ODT method of Claim 10, further comprising installing a second termination resistor in the synchronous memory device, the second termination resistor having one end connected to the data I/O port and the other end connected to the termination voltage port.

15. The ODT method of Claim 14, wherein a resistance value of the second termination resistor is remarkably larger than that of the first termination resistor.

16. The ODT method of Claim 10, further comprising generating the termination voltage using a voltage regulator, which is included in a system to which the synchronous memory device is attached, and supplying the termination voltage to the termination voltage port.

17. The ODT method of Claim 10, further comprising generating the termination voltage using a memory controller, which is included in a system to which the synchronous memory device is attached, and supplying the termination voltage to the termination voltage port.

18. A memory system comprising:

a memory controller;

a voltage regulator for generating a termination voltage; and

a synchronous memory device that is connected to the memory controller and the voltage regulator and includes an ODT circuit,

wherein the ODT circuit comprises:

a termination voltage port for receiving the termination voltage from the voltage regulator;

a data I/O port for receiving input data from the memory controller or outputting output data to the memory controller;

a first termination resistor, one end of which is connected to the data I/O port; and

a switch that selectively connects the other end of the first termination resistor to the termination voltage port in response to a termination enable signal.

19. The memory system of Claim 18, wherein the ODT circuit further comprises a termination enable signal generating circuit for generating the termination enable signal in response to a signal which indicates a valid section of input data or indicates that the present period is not a read period during write operations of the synchronous memory device, and for generating the termination enable signal in response to a signal output from an MRS.

20. The memory system of Claim 18, wherein the ODT circuit further comprises a second termination resistor, one end of which is connected to the data I/O port and the other end of which is connected to the termination voltage port.

21. A memory system comprising:

a memory controller for generating a termination voltage; and

a synchronous memory device that is connected to the memory controller and includes an ODT circuit,

wherein the ODT circuit comprises:

a termination voltage port for receiving the termination voltage from the memory controller;

a data I/O port for receiving input data from the memory controller or outputs output data to the memory controller;

a first termination resistor, one end of which is connected to the data I/O port; and

a switch that selectively connects the other end of the first termination resistor to the termination voltage port in response to a termination enable signal.

22. The memory system of Claim 21, wherein the ODT circuit further comprises a termination enable signal generating circuit for generating the termination enable signal in response to a signal which indicates a valid section of input data or indicates that the present period is not a read period during write operations of the synchronous memory device, and for generating the termination enable signal in response to a signal output from an MRS.

23. The memory system of Claim 21, wherein the ODT circuit further comprises a second termination resistor, one end of which is connected to the data I/O port and the other end of which is connected to the termination voltage port.

24. A memory system comprising:

a memory controller; and

a plurality of synchronous memory devices that are connected to the memory controller via a channel and include an ODT circuit,

wherein the ODT circuit is enabled in only at least one of the plurality of the memory devices that is furthest from the memory controller and is disabled in the other memory devices.

25. The memory system of Claim 24, wherein the ODT circuit comprises:

a termination voltage port for receiving a termination voltage;

a data I/O port;

a first termination resistor, one end of which is connected to the data I/O port; and

a switch that connects the termination voltage port to the other end of the first termination resistor in response to an activated termination enable signal,

wherein the termination enable signal is activated when an MRS installed in the memory device is set and the ODT circuit is enabled.